IN THE SPECIFICATION

Please amend the paragraph starting at page 14, line 22 of the application as follows:

FIGURE 3 illustrates exemplary power monitor circuit 300 according to an advantageous embodiment of the present invention. Power monitor circuit 300 comprises N-channel transistor 305, N-channel transistor 310, N-channel transistor 315, N-channel transistor 320, and capacitor 325. Power monitor circuit 300 further comprises three complementary metal-oxide-silicon (CMOS) inverters, that are serially connected to each other, and optional noise capacitor 335. CMOS inverter 330 comprises P-channel transistor 331 and N-channel transistor 332. CMOS inverter 340 comprises P-channel transistor 341 and N-channel transistor 342. Finally, CMOS inverter 350 comprises P-channel transistor 351 and N-channel transistor 352. The output of CMOS inverter 350 is the status signal (i.e., VALID) that cuts off DC current in power monitor circuit 300. As will be seen below, the VALID signal is an active low signal that goes low to indicate that VDDIO is powered up and goes high to indicate [[d]] that VDDIO is not powered up. As shown by the dashed lines in FIGURE 3, additional inverters 360, 370 could be used in the power monitor circuit 300, and the VALID signal would be produced by the inverter 370 rather than the inverter 350.

IN THE DRAWINGS

The Applicant proposes to amend Figure 3 to add two additional inverters 360 and 370. The Applicant has included a Letter to the Official Draftsperson showing the proposed changes in red ink.